

1 What is claimed is:

2 1. A method of operating an LCD display, the LCD display including pixels arranged in an
3 array of rows and columns, row driver circuitry for applying a row enable signal to a selected one of
4 the rows to enable the pixels within the selected row, and column driver circuitry for driving voltages
5 onto the columns of the LCD display for storage in the pixels of the selected row, the columns of the
6 LCD display including at least a first column located relatively proximate to the row driver circuitry
7 and at least a second column located relatively distant from the row driver circuitry, the row enable
8 signal being subject to a propagation delay as it is conducted along the selected row as measured
9 between the first column and the second column, the method comprising the steps of:

10 a. applying the row enable signal to a first selected row of the LCD display via the row
11 driver circuitry at a first predetermined time;

12 b. enabling a first column driver for applying a first driving voltage onto the first column of
13 the LCD display at a second predetermined time to transfer the first driving voltage onto a first pixel
14 located at an intersection of the first column with the first selected row;

15 c. enabling a second column driver for applying a second driving voltage onto the second
16 column of the LCD display at a third predetermined time to transfer the second driving voltage onto
17 a second pixel located at an intersection of the second column with the first selected row; and

18 d. delaying the third predetermined time beyond the second predetermined time by a delay
19 that is approximately equal to the propagation delay.

20
21 2. The method of claim 1 wherein each voltage driven onto a selected column of the LCD
22 display is also subject to a column propagation delay as it is conducted along the selected column as
23 measured between the column driver circuitry and a row relatively distant from the column driver
24 circuitry, the method further comprising the steps of:

25 e. applying a driving voltage onto the selected column of the LCD display at a first
26 predetermined time; and

27 f. enabling a row driver for applying the row enable signal to the row relatively distant
28 from the column driver at a second predetermined time delayed beyond the first predetermined time

1 by a delay that is approximately equal to the column propagation delay.

2
3 3. A method of operating an LCD display, the LCD display including pixels arranged in an
4 array of rows and columns, row driver circuitry for applying a row enable signal to a selected one of
5 the rows to enable the pixels within the selected row, and column driver circuitry for driving voltages
6 onto the columns of the LCD display for storage in the pixels of the selected row, the rows of the
7 LCD display including at least a first row located relatively proximate to the column driver circuitry
8 and at least a second row located relatively distant from the column driver circuitry, each voltage
9 driven onto each columns of the LCD display being subject to a column propagation delay as it is
10 conducted along the column as measured between the column driver circuitry and the second row,
11 the method comprising the steps of:

12 a. applying driving voltages onto the columns of the LCD display at a first predetermined
13 time; and

14 b. enabling a row driver for applying the row enable signal to the second row at a second
15 predetermined time delayed beyond the first predetermined time by a delay that is approximately
16 equal to the column propagation delay.

17
18 4. A method of compensating for propagation delay of a display line signal in a display
19 having display elements accessed by an array of row display lines and column display lines, the
20 method comprising the steps of:

21 a. generating a display line timing signal;

22 b. generating a first plurality of delayed display line timing signals in response to the
23 display line timing signal; and

24 c. activating one of at least one row display line and at least one column display line in
25 response to each of the first plurality of delayed display line timing signals.

26
27 5. The method of claim 4, wherein the step of generating a first plurality of delayed display
28 line timing signals comprises:

1 approximating a first propagation delay for the display line signal to propagate from its
2 source to a pixel associated with a first column display line; and
3 generating one of the first plurality of delayed display line timing signals to include a delay
4 substantially equal to the approximated first propagation delay for the display line signal.

5
6 6. The method of claim 4, further comprising the steps of:
7 generating a second plurality of delayed display line timing signals in response to one or
8 more of the first plurality of display line timing signals; and
9 activating one of the at least one row display line and at least one column display line in
10 response to each of the second plurality of delayed display line timing signals.

11
12 7. The method of claim 4, further comprising the steps of:
13 tracking which display line of a plurality of display lines is next to be activated;
14 selecting one of the first plurality of display line timing signals in response to the tracking of
15 which display line is next to be activated; and
16 activating a display line in response to the one of the first display line timing signals.

17
18 8. The method of claim 4, wherein the display line timing signal comprises signal
19 components to activate a plurality of display lines at varying times.

20
21 9. The method of claim 8, further comprising the step of generating a second plurality of
22 delayed display line timing signals in response to a first component of the display line timing signal.

23
24 10. The method of claim 9, further comprising the steps of:
25 removing the first component of the display line timing signal; and
26 generating a second plurality of delayed display line timing signals from a second component
27 of the display line timing signal.

1 11. The method of claim 9, further comprising activating at least one display line in response
2 to each of the second plurality of delayed display line timing signals.

3
4 12. A display line driver circuit for a display including display elements arranged in an array
5 of rows and columns, the display line driver circuitry generating display line timing signals, and
6 comprising:

7 a. a first plurality of delay elements operatively coupled together such that a signal
8 propagating through the first plurality of delay elements is increasingly delayed as it propagates
9 through each successive delay element;

10 b. a plurality of signal taps, each coupled between a selected pair of delay elements; and

11 c. at least one display line associated with each signal tap.
12

13 13. The display line driver circuit of claim 12 wherein each of the first plurality of delay
14 elements comprises at least one of a resistive and a capacitive element.
15

16 14. The display line driver circuit of claim 12 wherein the first plurality of delay elements
17 comprises a delay locked loop circuit.
18

19 15. The display line driver circuit of claim 12 wherein the display driver circuit is a column
20 driver circuit and the at least one display line comprises a plurality of column line groups each
21 associated with a column driver circuit.
22

23 16. The display line driver circuit of claim 15 further comprising a pulse generator coupled
24 to each signal tap.
25

26 17. The display line driver circuit of claim 16 wherein each pulse generator is coupled to its
27 respective signal tap through an inverter.
28

1 18. The display line driver circuit of claim 14 further comprising a delay locked loop
2 adjustment circuit.

3
4 19. The display line driver circuit of claim 18 wherein the delay locked loop circuit includes
5 an input and an output, and wherein the delay locked loop adjustment circuit comprises:
6 a calibration pulse generator coupled between an input of the delay locked loop circuit and a switch,
7 wherein the calibration pulse generator is configured to selectively activate the calibration circuit in
8 response to an input to the delay locked loop circuit;
9 a first comparator coupled to an output of the delay locked loop circuit;
10 a variable impedance element coupled between an inverting input of a second comparator and a first
11 reference voltage;
12 a first fixed impedance element coupled between a second reference voltage and a non-inverting
13 input to the second comparator and
14 a second fixed impedance coupled between the non-inverting input to of the second comparator and
15 the first reference voltage, wherein an output of the second comparator is coupled to an inverting
16 input of the first comparator.

17 a. a calibration pulse generator coupled to the input of the delay locked loop circuit;

18 b. a first comparator having an inverting input, a non-inverting input, and an output, the
19 non-inverting input being coupled to the output of the delay locked loop circuit;

20 c. a second comparator having an inverting input, a non-inverting input, and an output, the
21 output of the second comparator being coupled to the inverting input of the first comparator;

22 d. a variable impedance element coupled between the inverting input of the second
23 comparator and a first reference voltage;

24 e. a first impedance element coupled between a second reference voltage and the non-
25 inverting input of the second comparator; and

26 f. a second fixed impedance coupled between the non-inverting input of the second
27 comparator and the first reference voltage.

1 20. The display line driver circuit of claim 18 wherein the delay locked loop adjustment
2 circuit comprises a variable resistor coupled in parallel with a capacitor.

3
4 21. The display line driver circuit of claim 20 wherein the delay locked loop adjustment
5 circuit includes a variable resistance, the delay locked loop adjustment circuit being configured to
6 increase a relative delay of the delay elements as the variable resistance is increased, and to decrease
7 the relative delay of the delay elements as the variable resistance is decreased.

8
9 22. The display line driver circuit of claim 15, wherein each column line driver group circuit
10 comprises:

11 a. a second plurality of successive delay elements operatively coupled together such that a
12 signal propagating through the second plurality of delay elements is increasingly delayed as it
13 propagates through each successive delay element;

14 b. a plurality of signal taps each coupled between a selected pair of successive delay
15 elements within the second plurality of successive delay elements; and

16 c. at least one column signal line associated with each signal tap.

17
18 23. The display line driver circuit of claim 12 wherein the display line driver circuit is a row
19 driver circuit, and wherein the at least one display line associated with each signal tap includes a
20 plurality of row line groups, each of the plurality of row line groups being associated with a signal
21 tap, and each of the plurality of row line groups having a plurality of row lines associated therewith.

22
23 24. The display driver of claim 23, wherein the row driver circuit sequentially initiates each
24 row of each plurality of row lines with a signal having a delay corresponding to the row line group
25 with which it is associated.

26
27 25. The display driver of claim 24, further comprising a row counter circuit for tracking the
28 sequential initiation of row lines and for selecting an appropriate signal tap through which a row

1 initiation signal is to be received for each row line.
2

3 26. A display having pixels arranged in an array of rows and columns, row driver circuitry
4 for applying a row enable signal to a selected one of the rows to enable the pixels within the selected
5 row, and column driver circuitry for driving voltages onto the columns of the display for storage in
6 the pixels of the selected row, the columns of the display including at least a first column located
7 relatively proximate to the row driver circuitry and at least a second column located relatively distant
8 from the row driver circuitry, the row enable signal being subject to a propagation delay as it is
9 conducted along the selected row as measured between the first column and the second column, the
10 display comprising:

- 11 a. a first plurality of delay elements within the column driver circuitry which are
12 operatively coupled together such that a signal propagating through the first plurality of delay
13 elements is increasingly delayed as it propagates through each successive delay element; and
14 b. a signal tap associated with the second column coupled at a selected point between two
15 of the delay elements such that the delay of the signal propagating through the first plurality of delay
16 elements at that selected point is substantially equal to the propagation delay of the row enable signal
17 when it reaches the second column.
18

19 27. The display of claim 26, wherein the first plurality of delay elements comprises at least
20 one element selected from the group of elements that includes resistive and capacitive elements.
21

22 28. The display of claim 26, wherein the first plurality of delay elements comprises a delay
23 locked loop circuit.
24

25 29. The display of claim 26 further comprising a group of columns associated with a column
26 group driver circuit for driving voltages onto each column of the group, said group of columns
27 including the second column.
28

1 30. The display of claim 29 further comprising a first pulse generator coupled to the signal
2 tap.

3
4 31. The display of claim 30 further comprising a second pulse generator coupled to the
5 signal tap through an inverter.

6
7 32. The display of claim 29 further comprising a delay locked loop adjustment circuit.

8
9 33. The display of claim 32 wherein the delay locked loop adjustment circuit comprises:

- 10 a. a calibration pulse generator coupled to the input of the delay locked loop circuit;
- 11 b. a first comparator having an inverting input, a non-inverting input, and an output, the
12 non-inverting input being coupled to the output of the delay locked loop circuit;
- 13 c. a second comparator having an inverting input, a non-inverting input, and an output, the
14 output of the second comparator being coupled to the inverting input of the first comparator;
- 15 d. a variable impedance element coupled between the inverting input of the second
16 comparator and a first reference voltage;
- 17 e. a first impedance element coupled between a second reference voltage and the non-
18 inverting input of the second comparator; and
- 19 f. a second fixed impedance coupled between the non-inverting input of the second
20 comparator and the first reference voltage.

21
22 34. The display of claim 32 wherein the delay locked loop adjustment circuit comprises a
23 variable resistor coupled in parallel with a fixed capacitor.

24
25 35. The display of claim 34 wherein the delay locked loop adjustment circuit includes a
26 variable resistance, the delay locked loop adjustment circuit being configured to increase a relative
27 delay of the delay elements as the resistance of the variable resistor is increased, and to decrease the
28 relative delay of the delay elements as the resistance of the variable resistor is decreased.

1 36. The display of claim 29, wherein the column driver group circuit comprises:

2 a. a second plurality of successive delay elements operatively coupled together such that a
3 signal propagating through the second plurality of delay elements is increasingly delayed as it
4 propagates through each successive delay element;

5 b. a signal tap associated with a third column among the column group and coupled at a
6 selected point between two of the successive delay elements within the second plurality of successive
7 delay elements; such that the delay of the signal propagating through the second plurality of
8 successive delay elements at that selected point is substantially equal to the propagation delay of the
9 row enable signal when it reaches the third column.

10
11 37. The display of claim 26 wherein the row driver circuitry is configured to sequentially
12 initiate each row associated with the row driver circuitry at predetermined intervals, the row driver
13 circuitry having associated therewith at least a first row located relatively proximate to the column
14 driver circuitry and at least a second row located relatively distant from the column driver circuitry,
15 each voltage driven onto a column being subject to a propagation delay as it is conducted along the
16 selected column as measured between the first row and the second row, the display further
17 comprising:

18 a. a plurality of successive row signal delay elements within the row driver circuitry which
19 are operatively coupled together such that a signal propagating through the plurality of successive
20 row signal delay elements is increasingly delayed as it propagates through each successive row delay
21 element;

22 b. a plurality of signal taps associated with selected points among the plurality of
23 successive row signal delay elements; and

24 c. circuitry configured to select a first signal tap from among the plurality of signal taps
25 which will approximate the propagation delay of the voltage driven onto a column as it reaches the
26 second row.

27
28 38. A display signal timing controller for a display having a plurality of display elements

1 arranged in an array of rows and columns, row driver circuitry for applying a row enable signal to a
2 selected one of the rows in response to a row timing signal, the row enable signal being subject to a
3 propagation delay as it is conducted along the row, and column driver circuitry for driving voltages
4 onto the columns of the display for storage in the pixels of the selected row in response to a column
5 timing signal, the voltage driven onto the column also being subject to a propagation delay as it is
6 conducted along the column, the display signal timing controller comprising:

- 7 a. a plurality of delay elements coupled in series for delaying a first display timing signal;
- 8 b. a plurality of taps coupled between select delay elements of the plurality of delay
9 elements for tapping delayed portions of the first display timing signal; and
- 10 c. output circuitry configured to generate a second display timing signal in response to the
11 first display timing signal, the second display timing signal having signal components corresponding
12 to each of the delayed portions of the tapped first display timing signal.

13
14 39. The display signal timing controller of claim 38 further comprising a plurality of display
15 driver circuits, wherein each of the display driver circuits comprises:

- 16 a. input circuitry configured to generate a third display timing signal in response to a signal
17 component of the second display timing signal;
- 18 b. a second plurality of delay elements for delaying the third display timing signal; and
- 19 c. a plurality of taps coupled between select delay elements of the second plurality of delay
20 elements for tapping delayed portions of the third display timing signal.

21
22 40. A display having pixels arranged in an array of rows and columns, row driver circuitry
23 for applying a row enable signal to a selected one of the rows to enable the pixels within the selected
24 row, and column driver circuitry for driving voltages onto the columns of the display for storage in
25 the pixels of the selected row, the rows of the display including at least a first row located relatively
26 proximate to the column driver circuitry and at least a second row located relatively distant from the
27 column driver circuitry, each voltage driven onto a column being subject to a propagation delay as it
28 is conducted along the column as measured between the first row and the second row, the display

1 comprising:

2 a. a plurality of successive row signal delay elements within the row driver circuitry which
3 are operatively coupled together such that a signal propagating through the plurality of successive
4 row signal delay elements is increasingly delayed as it propagates through each successive row signal
5 delay element;

6 b. a plurality of signal taps associated with selected points among the plurality of
7 successive row signal delay elements; and

8 c. circuitry configured to select a first signal tap from among the plurality of signal taps
9 which will approximate the propagation delay of the voltage driven onto a column as it reaches the
10 second row.